

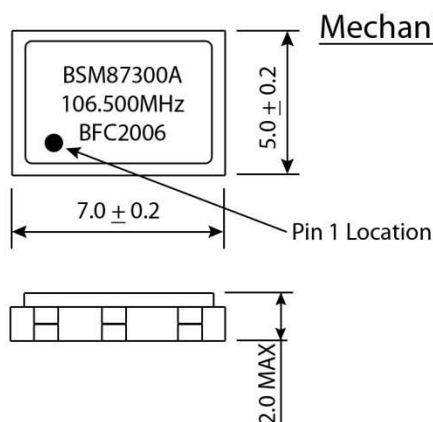


**Features:**

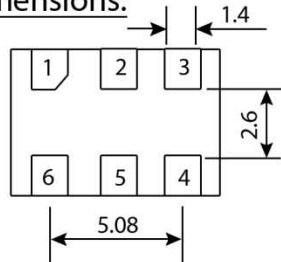
- **RoHS Compliant** , Best Suited for ECL Logic Devices
- Very Low Phase Jitter, Excellent Noise Margin, No Internal PLL
- Leadless Chip Carrier (LCC) Ultra Small Package, Industry de Facto Standard Footprint
- Complimentary Output, Tri-State Enable/Disable Standard or Option

ELECTRICAL SPECIFICATIONS			
Frequency Range (MHz)	10.0 to 320 MHz		
Standard Frequency	10 MHz / 15.625 MHz / 19.53125 MHz / 80 MHz / 100 MHz / 106.25 MHz / 125 MHz / 133.33 MHz / 155.52 MHz / 156.25 MHz / 161.1328 MHz		
Input Voltage (Vcc)	+3.3 VDC $\pm$ 0.3 VDC	+2.5 VDC $\pm$ 5%	
Overall Frequency Stability	$\pm$ 100ppm	$\pm$ 50ppm	$\pm$ 25ppm
Temperature Range	0°C to +70°C		-40°C to +85°C
Standard Stability	$\pm$ 50ppm / 0°C to 70°C		
Electric Option (Duty Cycle)	Tristate 60/40%; Tristate 55/45%; Tristate 52.5/47.5%; No Tristate 60/40%; No Tristate 55/45%; No Tristate 52.5/47.5%		
Output Load	50 Ohms to Vcc – 2V Thevenin Equivalent, Bias Required		
Logic "1" / Logic "0" Level	(Vcc -1.02V) Min. / (Vcc -1.63) Max		
Rise and Fall Time (Tr/Tf)	1 ns Max. Measured Between 20% to 80% Vp-p		
Start Up Time	5 ms Max.		
Phase Jitter (RMS, 1 Sigma)	1 ps Max. fj > 1 kHz; 0.3 ps fj = 12 kHz to 20 MHz		
Tristate Function	Input (Pin 1) High (>0.7 Vcc) or Open: Output (Pin 4,5) Active Input (Pin 1) Low (<0.3 Vcc) or Open: Output Disabled in High Impedance		
Enable / Disable Time	100 ns Maximum		

Part Number Table					
Model	Input Voltage	Stability	Symmetry (Tristate)	Temp. Range (°C)	Frequency
BSM88P	3 = +3.3 VDC $\pm$ 5%	B = $\pm$ 100ppm	S = 55/45	Blank = 0° to 70°C	In MHz
	2 = +2.5 VDC $\pm$ 5%	C = $\pm$ 50ppm	Blank = 60/40	M = -40° to 85°C	
		E = $\pm$ 25ppm	ST = 52.5 / 47.5		

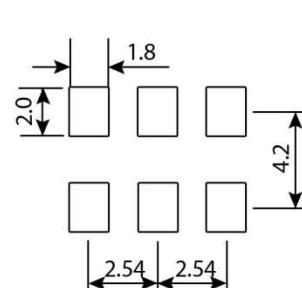


**Mechanical Dimensions:**



Pin Connections  
 #1: E/D or NC      #2: N/C  
 #3: Ground, Case    #4: Output  
 #5: Complie-Output   #6: Vcc

**Recommended Solder Pad Layout**



All dimensions are typical unless otherwise specified

Dimensions in Millimeters